16. (Amended) A transistor comprising according to claim [11] 15, wherein each of the n^- impurity regions has a depth not deeper 50 [μm] nm.

REMARKS

The Official Action Mailed November 30, 1999 has been received and its contents carefully noted. Claims 1-16 are pending in the present application and claims 12-14 and 16 are amended. For the reasons discussed in detail below, the present application is believed to be in condition for allowance and favorable reconsideration of the outstanding rejections is requested.

Initially, the specification has been amended to update the copendency statement. Specifically, parent application serial number 08/847,314 now includes reference to issued U.S. Patent 5,965,915 as requested in the Official Action. Furthermore, although not requested in the Official Action, application serial number 08/692,227 has been updated to refer to issued U.S. Patent 5,789,292.

Claims 11-16 are rejected under 35 U.S.C. § 112, second paragraph, and claims 12, 14, and 16 are rejected under 35 U.S.C. §112, first paragraph. In response, Applicants have amended claims 12-14 and 16 as suggested in the Official Action and reconsideration is requested in view thereof.

Claims 1-10 are rejected under the doctrine of double patenting based on U.S. Patent 5,965,915 (which issued from application serial number 08/847,314, as noted above). In response, a Terminal Disclaimer will be filed to obviate this rejection as soon as the original executed copy is received from Japan. With the filing of this Terminal Disclaimer, this rejection is believed to be overcome and favorable reconsideration is requested.

Claims 11-16 have been rejected under 35 U.S.C. §103 as being unpatentable over Yoshitomi et al. (U.S. Patent 5,434,440). Additionally, claims 11-16 are rejected under 35 U.S.C. §103 as being unpatentable over Chou et al. (U.S. Patent 5,565,700).

The claimed invention is characterized in a memory device with a drain region having a depth shallower than a source region and not deeper than 0.1 μm, and a transistor with a channel region having a length not longer than 0.3 μm.

Applicants submit that both Yoshitomi and Chou do not teach a channel length but a gate length. Yoshitomi discloses a p-channel MOSFET having a gate length Lg of 0.15 μm

(col. 10, lines 53-54). However, as shown in Figs. 4A-4D, and 8A-8D, the impurities are diffused so that the gate length does not coincide with the channel length. Applicants further submit that Chou also teaches a gate length between about 0.1 to 5 μm (col. 2, lines 44-45). In Figs. 1-6, lightly doped source and drain regions are dispersed under the gate electrode. Therefore, Chou's gate length is not the same as the channel length. For at least this reason, it is respectfully submitted that the claims of the present application are not obvious in view of the cited prior art and favorable reconsideration is respectfully requested.

Applicants would also respectfully request that the Examiner acknowledge and initial the PTO-1449 form filed with the Information Disclosure Statement on December 21, 1999.

For all of the above reasons, the present application is believed to be in condition for allowance. If the Examiner has any further questions, he is invited to contact the undersigned.

Respectfully submitted,

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